REMARKS

In response to the Examiner's Action mailed April 4, 2002, Applicants amend their application and request reconsideration. In this Amendment, claims 1-3, 5, 8, 9, and 11-13 are cancelled, leaving examined claims 4, 6, and 7 pending.

Claim 7 was rejected as not supported by the application as filed. The Examiner asserted that claim 7 had been broadened in the previous Amendment. Applicants respectfully disagree. The amendment of claim 7 in the previous response was intended solely to eliminate the alternative limitation, i.e., "or". Perhaps the words "at least" should not have been added to claim 7 and those are removed here so that the scope of claim 7 is identical to the scope of claim 7 as originally filed. Therefore, the rejection of claim 7 should now be withdrawn.

Claims 1-9 and 11-13 were rejected as unpatentable over Tsutsui (U. S. Patent 5,925,901) in view of Tozawa (Japanese Published Patent Application Hei. 3-270024), and further in view of Taguchi (U. S. Patent 5,001,108) and Kobayashi (Japanese Published Patent Application 61-232682). This rejection is respectfully traversed as to the claims remaining, namely, claims 4, 6, and 7.

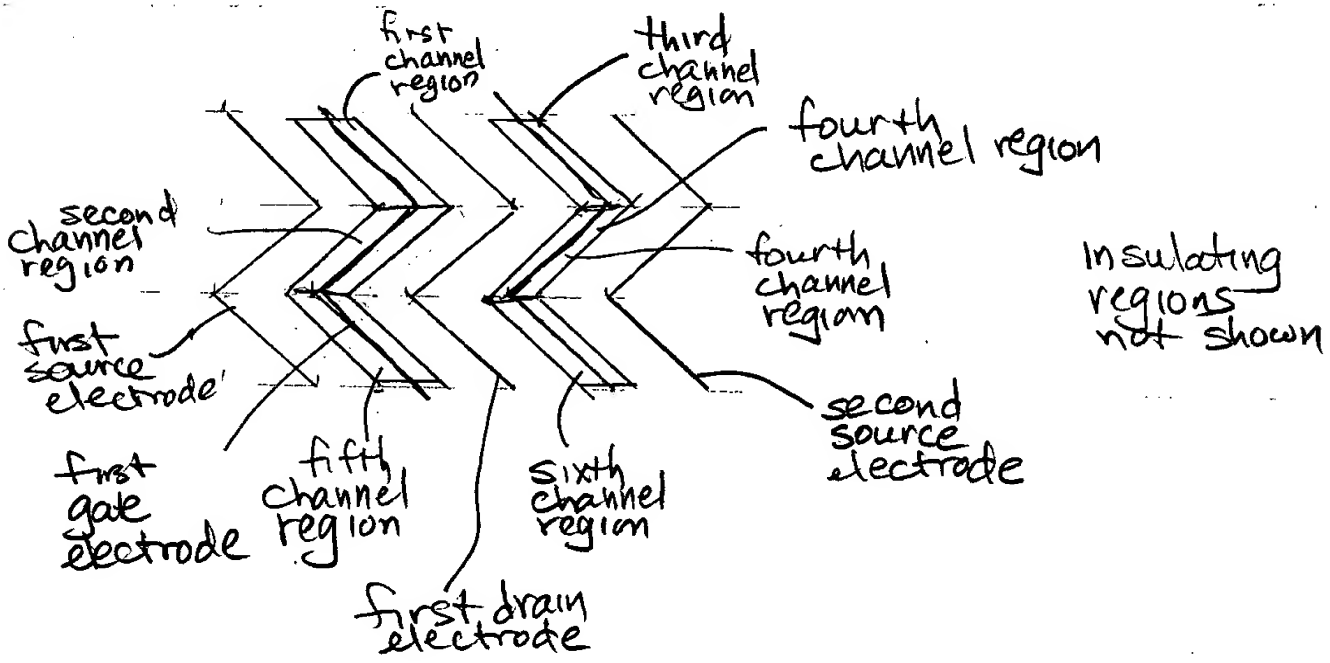
While Applicants do not rely upon the electrical nature of the compound semiconductor substrate to demonstrate the patentability of the claims remaining upon entry of this Amendment, the Examiner's reliance upon Taguchi as pertinent prior art, "form the same filed of endeavor", is erroneous. Taguchi relates to the use of a *superconductor* in a semiconductor device to reduce the resistance of wiring to essentially zero at low temperatures. That purpose has nothing to do with the invention although Taguchi relates to highly specialized field effect transistors.

In this Amendment, claims 4 and 6 have been written in independent form, retaining their original numbering. The combination of the claims is somewhat awkward but not a single word, with the exception of an obvious error that is corrected here, has been changed in making the claim combination to ensure that no new issue is raised in the claim combinations. The change that has been made in each of the claims involved changing the word "being" to "bending", the obviously intended word that appears elsewhere in the claims.

Claims 4 and 6 both encompass the structure illustrated in Figure 4 of the patent application. It is presumed that the Examiner understands the claims as describing a first source electrode and a first drain electrode, each of which includes two bending positions and a gate electrode that likewise includes a similar number of bending positions. As shown in the embodiment of Figure 4, these electrodes are all aligned in rows. Insulating films 14a extend in stripes along the active region of the compound semiconductor substrate and pass beneath the bending positions of each of the electrodes.

In commenting on claims 4 and 6, the Examiner referred to Tsutsui at column 3, lines 59-64, and six sets of FETs with six sets of channels and the connections as shown in Figures 7 and 8 of Tsutsui. This description indicates that the Examiner may nor have properly interpreted the claim language. For that reason, the following sketch is provided, not as a limitation of the claims but to illustrate the proper interpretation of the claims in accordance with the embodiment of Figure 4 of the patent application.

The fact that the structure shown in Figure 7 of Tsutsui includes six gate electrodes in each field effect transistor unit is not pertinent to the claim language. The claim language is directed to a structure including two gate electrodes each having three parts, i.e., six gate electrode parts, not six gate electrodes in one unit, as in Figure 7 of Tsutsui. Thus, the proposition for which Tsutsui was cited in rejecting claims 4 and 6 is not entirely clear since it is understood that Kobayashi and Tozawa are relied upon as disclosing field effect transistor structures in which gate electrodes have multiple parts with bends between the parts. Hopefully, the sketch will assist in proper interpretation of the claims.



Each of claims 4 and 6 recites first and second insulating regions on the semiconductor substrate under the respective bends of the gate electrodes. In the embodiment of Figure 4, the insulating films 14a are stripes extending along the active region under the bending positions of each of the gate electrodes. In rejecting claims 4 and 6, the Examiner referred to Figures 7 and 8 of Tsutsui, asserting that there are first and second insulating regions on the semiconductor substrate under the bending regions of the gate electrodes. This interpretation of Tsutsui is difficult to understand for several reasons. Moreover, the interpretation is contrary to what is claimed in the patent application and, therefore, cannot establish *prima facie* obviousness of claims 4 and 6.

According to column 4, lines 3 and 31, of Tsutsui, the active region In Tsutsui's Figure 7 is the region 2 and that active region 2 is surrounded by an insulation region formed by ion implantation. The gate electrodes Gf in each unit of the four units illustrated in Figure 7 of Tsutsui all connect to a gate bar Gb. It is presumed that the Examiner is considering that the gate electrode bends referred to in claims 4 and 6 correspond to the junctions between the gate electrode fingers Gf and the gate bar Gb in Figure 7 of Tsutsui. Applicants respectfully disagree with this interpretation for two independent reasons.

First, in the claimed invention as defined by claims 4 and 6, each gate electrode includes two ninety degree bends. It is readily apparent that, in Tsutsui, the gate electrodes are the gate fingers Gf and that each gate finger is free of bends. Second, even if the potential interpretation by the Examiner concerning the bends in the gate electrodes is accepted, it is apparent that the bends occur in Figure 7 of Tsutsui *outside* the active region 2. By contrast, in the invention, as defined in paragraph (c) of claims 4 and 6, the first semiconductor element is in the active region and includes the first and third bending positions. Likewise, in the invention, the second semiconductor element includes "on the active region" the second gate electrode which is bent at the second and fourth bending positions. Thus, the claim clearly defines the positions where the first and second gate electrodes are bent as being within the active region of the substrate with the insulating regions beneath the bending portions in the active region, quite unlike Tsutsui or anything illustrated in Kobayashi or Tozawa. No parts of the gate electrodes in the references include, in the active region, insulators separating the bending positions of the gate electrodes from the substrate.

A fundamental requirement for establishing *prima facie* obviousness is that all of the elements of a claim so rejected must be present in the sources of prior art sought to be combined to meet the claim limitations. That requirement is not met here because no

reference discloses gate electrodes with multiple bends within the active region of the structure with insulating regions beneath those bending portions in the active region of the semiconductor substrate.

Since, in this Amendment, claims are only combined and cancelled, and claim 7 is amended to overcome a rejection as to form, no new issues can be raised by this Amendment. Therefore, even if the Examiner intends to maintain the rejection, the Amendment should be entered to place the application in better form for appeal. However, since the remaining claims clearly distinguish from the prior art applied in rejecting the claims, upon entry of the Amendment, a Notice of Allowance should be issued as to claims 4, 6, and 7.

Respectfully submitted,

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PATENT
Attorney Docket No. 400762/Aoyama

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

SUZUKI et al.

Application No.:	09/613,749	Art Unit:	2814
Filed:	July 11, 2000	Examiner:	S. Rao
For:	FIELD EFFECT TRANSISTOR STRUCTURE WITH BENT GATE		

SPECIFICATION, CLAIMS, AND ABSTRACT AS AMENDED IN RESPONSE TO THE OFFICIAL ACTION MAILED APRIL 4, 2002

Amendments to existing claims:

4. (Thrice Amended) ~~The~~A semiconductor device ~~according to claim 1,~~ comprising:

(a) an electrically isotropic compound semiconductor substrate having a first surface and a second surface;

(b) an active region on the first surface of the substrate;

(c) a first semiconductor element in the active region, including

first and second channel regions having width directions essentially perpendicular to each other,

a first source electrode and a first drain electrode, adjacent to the first and second channel regions and opposing each other with the first and second channel regions therebetween, and in ohmic contact with the active region,

a first gate electrode on the first and second channel regions and along the first source electrode and the first drain electrode, and bent at at least one bending position; and

a fifth channel region joining the second channel region and having a width direction essentially perpendicular to the width direction of the second channel region, wherein the first gate electrode is disposed on the first, second, and fifth channel regions and is bent at the first bending position and at a third bending position; and

(d) a second semiconductor element on the active region adjacent to the first semiconductor element, including

third and fourth channel regions adjacent to the first and second channel regions, respectively, with one of the first source electrode and the first drain electrode therebetween,

one of a second source electrode and a second drain electrode opposing the first drain electrode or the first source electrode across the third and fourth channel regions, and in ohmic contact with the active region,

a second gate electrode on the third and fourth channel regions and along one of the second source electrode and the second drain electrode, and bent at at least one bending position; and

a sixth channel region joining the fourth channel region and having a width direction essentially perpendicular to the width direction of the fourth channel region, wherein the second gate electrode is disposed on the third, fourth, and sixth channel regions and is bent at the second bending position and at a fourth ~~being~~ bending position; and

(e) first and second insulating regions on the semiconductor substrate and under the first and second bending positions of the first and second gate electrodes, and under the third and fourth bending positions of the first and second gate electrodes, respectively.

6. (Thrice Amended) ~~The~~A semiconductor device ~~according to claim 5,~~ comprising:

(a) an electrically isotropic compound semiconductor substrate having a first surface and a second surface;

(b) an active region on the first surface of the substrate;

(c) a first semiconductor element in the active region, including

first and second channel regions having width directions essentially perpendicular to each other,

a first source electrode and a first drain electrode, adjacent to the first and second channel regions and opposing each other with the first and second channel regions therebetween, and in ohmic contact with the active region, wherein the first source electrode has a rectangular shape, two sides of which are adjacent to the first and second channel regions, respectively, and wherein the first source electrode is

connected to a conductive film on the second surface of the semiconductor substrate through a via-hole in the first source electrode,

a first gate electrode on the first and second channel regions and along the first source electrode and the first drain electrode, and bent at at least one bending position; and

a fifth channel region joining the second channel region and having a width direction essentially perpendicular to the width direction of the second channel region, wherein the first gate electrode is disposed on the first, second, and fifth channel regions and is bent at the first bending position and at a third bending position; and

(d) a second semiconductor element on the active region adjacent to the first semiconductor element, including

third and fourth channel regions adjacent to the first and second channel regions, respectively, with one of the first source electrode and the first drain electrode therebetween,

one of a second source electrode and a second drain electrode opposing the first drain electrode or the first source electrode across the third and fourth channel regions, and in ohmic contact with the active region,

a second gate electrode on the third and fourth channel regions and along one of the second source electrode and the second drain electrode, and bent at at least one bending position; and

a sixth channel region joining the fourth channel region and having a width direction essentially perpendicular to the width direction of the fourth channel region, wherein the second gate electrode is disposed on the third, fourth, and sixth channel regions and is bent at the second bending position and at a fourth ~~being~~ bending position; and

(e) first and second insulating regions on the semiconductor substrate and under the first and second bending positions of the first and second gate electrodes, and under the third and fourth bending positions of the first and second gate electrodes, respectively.

7. (Thrice Amended) The semiconductor device according to claim 6, wherein the width of ~~at least~~ one of the first and second channel regions is narrower than the width of the source electrode adjacent the channel region.